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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/777,097	02/13/2004	Jae-jun Moon	Q77183	4555

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EXAMINER	
ZWEIZIG, JEFFERY SHAWN	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 08/18/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/777,097	MOON ET AL.	
	Examiner	Art Unit	
	Jeffrey S. Zweizig	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 July 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☒ Claim(s) *4* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 July 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *6/14/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Claim Objection

1. In claim 4 line 13, "a second common node" should be --the second common node--.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1, 3 and 5-9 are rejected under 35 U.S.C. 102(b) as being anticipated by Wu et al. (USPN 5,307,007).

As pointed out in the previous Office Action, Fig. 1 discloses a bias circuit part M1-M4/R1, an output node (node between M1 & M3), a start-up capacitor C1, a common node (gates of M1/M2) and MOS transistors M1/M2 as recited in claim 1.

As pointed out in the previous Office Action, Fig. 3 discloses a bias circuit M1-M8/R1, an output node (node between M5 & M7, a first common node (gates of M3/M4), first MOS transistors M3 & M4, a second common node (gates of M5/M6), second MOS transistors M5 & M6, a fist capacitor C1 and a second capacitor C2 as recited in claim 3.

The output node outputs the constant bias voltage to another circuit outside the bias circuit (wherein M5 and M6 are seen as the another circuit outside the bias circuit) as recited in new claims 5 and 7.

The output node outputs the constant bias voltage to another circuit outside the bias circuit (wherein M9 and M10 are seen as the another circuit outside the bias circuit) as recited in new claims 6 and 8.

New claims 9 is seen to be the same as existing claim 1 wherein "output node" has been replaced with "output terminal" and "base of the output terminal". No patentable difference is seen to exist between these three phrases. Claim 9 is anticipated for the reasons above.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamazaki (5,180,967) in view of Wu et al. (5,307,007).

Yamazaki Fig. 1 discloses a bias circuit part 104/106/110/112/114, an output node (N11 or N12), a common node (gates of 104/106) and MOS transistors 104/106 as recited in claim 1. Further shown are start-up circuits 118 & 120. Not shown is a

start-up capacitor as recited in claim 1. As indicated in the 102 rejections above, Wu et al. Fig. 1 (as well as Figs. 2, 4 & 6) disclose similar bias circuit parts including an output node, a common node and MOS transistors as well as start up capacitors C1 and C2. It would have been obvious to one of ordinary skill in the art at the time of the invention to replace the Yamazaki start-up circuits 118 & 120 with a start-up capacitor as taught by Wu et al. for the benefit of reducing component count and static current consumption. Claim 1 is obvious.

Yamazaki Fig. 1 further discloses a first PMOS 106, a second PMOS 104, a first NMOS 110, a second NMOS 112 and a resistor 114 as recited in claim 2. Both N11 and N12 are valid output nodes. Yamazaki extracts a signal from the output node between the second PMOS transistor 104 and the second NMOS transistor 112, however, Wu et al. Fig. 1 shows that a signal can just as well be extracted from the output node between the first PMOS transistor M1 and the first NMOS transistor M3. Claim 2 is obvious.

Yamazaki Fig. 5 discloses a bias circuit 104/106/124/126/130/128/114, an output node (nodes between 126 & 110 or between 124 &112), first MOS transistors 104 & 106 and second MOS transistors 124 & 126 as recited in claim 3. Further shown are start-up circuits 118 & 120. Not shown are start-up capacitors as recited in claim 3. As indicated in the 102 rejections above, Wu et al. Fig. 3 (as well as Fig. 5) disclose similar bias circuits including an output node, and MOS transistors as well as start up capacitors C1 and C2. It would have been obvious to one of ordinary skill in the art at the time of the invention to replace the Yamazaki start-up circuits 118 & 120 with start-

up capacitors as taught by Wu et al. for the benefit of reducing static current consumption. Claim 3 is obvious.

Yamazaki Fig. 5 further discloses a first PMOS 106, a second PMOS 104, a third PMOS 126, a fourth PMOS 124, a first NMOS 110, a second NMOS 112 and a resistor 114 as recited in claim 4. Nodes between 126 & 110 or between 124 &112 are all valid output nodes. For example, Wu et al. Fig. 3 shows that a signal can be extracted from an output node formed by the drain of the first NMOS transistor M7. Claim 4 is obvious.

The output node outputs the constant bias voltage to another circuit outside the bias circuit (wherein 116 (or M5 and M6 from Wu et al.) are seen as the another circuit outside the bias circuit) as recited in new claims 5 and 7.

The output node outputs the constant bias voltage to another circuit outside the bias circuit (wherein 116 (or M9 and M10 from Wu et al.) are seen as the another circuit outside the bias circuit) as recited in new claims 6 and 8.

New claims 9 and 10 are seen to be the same as existing claims 1 and 2 wherein "output node" has been replaced with "output terminal" and "base of the output terminal". No patentable difference is seen to exist between these three phrases. Claims 9 and 10 are obvious for the reasons above.

Response to Amendments and Arguments

6. All 112 rejections are withdrawn in light of Applicant's amendments. The drawing amendments are also acceptable. Of course the output nodes were implied in Fig. 13 and 14. Just as they are implied in Examiner's relied upon references. Examiner is

dropping the issue of Figs. 13 and 14 so as not to clutter the present prosecution, which appears to be headed for Appeal.

Likewise, Examiner is dropping the 103 rejection in connection with Wu et al. in view of Applicant's Prior Art Fig. 1 and Yamazaki. The rejection is being dropped because it was redundant. The remaining rejections stand on their own and will make for a more concise Appeal.

None of Applicant's arguments are persuasive. Refer to Wu et al. Fig. 1, for example. One of ordinary skill in the art would recognize this circuit as comprising several common definable stages. Transistors M5 and M6, for example, form simple voltage-to-current converters for receiving a bias voltage from circuit M1-M4 and providing currents to regulator 40. That is, circuit M1-M4 outputs a signal that is received by circuits M5 and M6. Therefore the connection is seen as an output node (or output terminal or base of an output terminal) from M1-M4.

Alternatively, referring to the Wu et al. reference again, Fig. 1 shows a transistor M3 with a drain and gate connected to the drain of transistor M1. This connection is called a node. Note the small dots that define this connection, which are often referred to by those of ordinary skill in the art as "node dots". The connection between transistors M1 and M3 provides a signal to the gates of transistors M5 and M6. Provide is another word for output. In other words, a signal is output from the node connecting M1 and M3. Those of ordinary skill in the art would refer to such a node as an "output node" or an "output terminal" or a "base of an output terminal". No patentable distinction is seen to exist between any of these terms.

Conclusion

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeffrey S. Zweizig whose telephone number is (571) 272-1758. The examiner can normally be reached on Monday thru Wednesday 6:00 am to 6:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy P. Callahan can be reached on (571) 272-1740. The fax phone

number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Jeffrey S. Zweizig
Primary Examiner
Art Unit 2816

FIG. 12

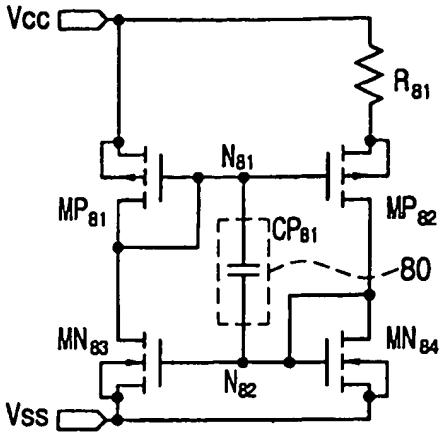

FIG. 13

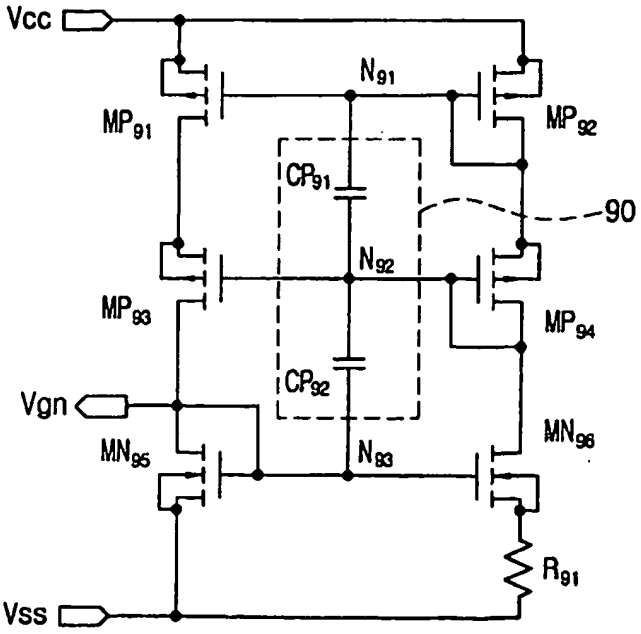

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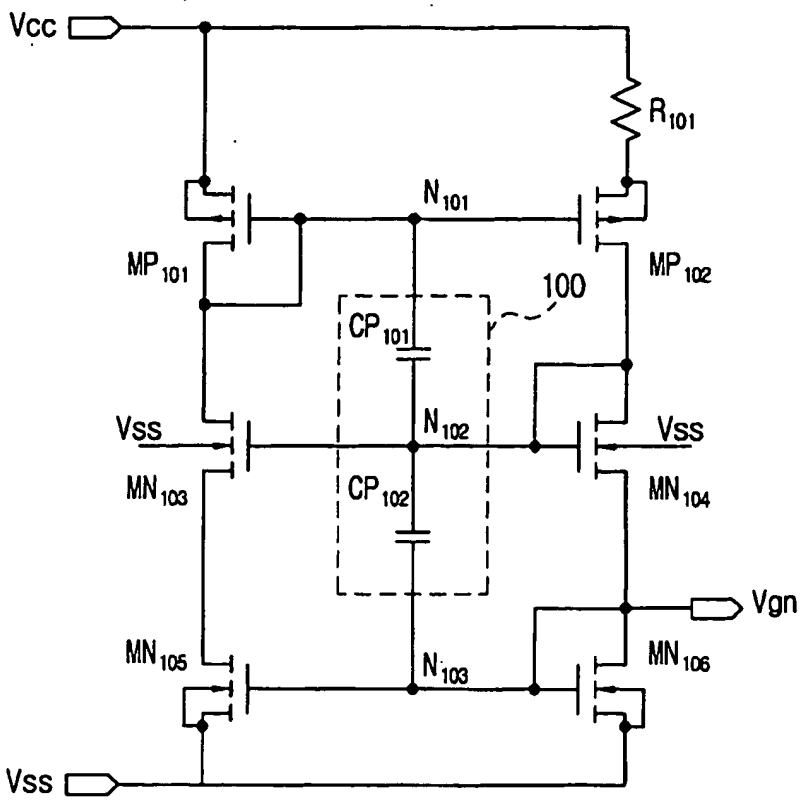
FIG. 14



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